A Packaged 20-GHz 1-W GaAs MESFET with a Novel Via-Hole Plated Heat Sink Structure

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Abstract—A novel Via-Hole plated heat sink (PHS) structure with an improved gate-packing density is developed for *K*-band GaAs power FET's. The gate-packing density in this structure is increased to four times greater than that in the conventional direct via-hole structure, by making via-holes under the source-grounding pads fabricated outside the FET active area. The increase in the gate-packing density allows the design of a high-power, high-frequency FET with a larger gate periphery. The resultant 2.4-mm gate periphery device with 0.7-μm gate length delivered 1.1 W (30.4 dBm) of output power with 5.0-dB gain and 19.2-percent power added efficiency at 20 GHz, and exhibited 0.74 W (28.7 dBm) at 30 GHz. The same type of device assembled in the hermetically sealed package delivered 1.0 W (30 dBm) of output power with 4.8-dB gain and 13-percent power added efficiency at 20 GHz. Thermal- and mechanical-environmental tests were made to assess the reliability of the novel Via-Hole PHS FET. Results showed no failure nor significant change in device parameters throughout the tests.

I. INTRODUCTION

IT IS WELL KNOWN that in order to get the sufficient power gain at higher frequency bands, it is important not only to improve intrinsic FET parameters, but also to reduce parasitic elements such as source-inductance L_s. The so-called via-hole plated heat sink (PHS) structure has been widely used for this purpose.

The concept of a via-hole structure in FET's was first proposed by Fukuta in 1972 [1]. In 1975, a large reduction in the common-lead source inductance of FET's was confirmed by the method of via-connections through a semi-insulating substrate [2]. In 1977, D'Asaro *et al.* [3], [4] realized 4-GHz transistors made with via-connections to sources, which successfully improved the gain by the factor of 2 dB or more at small-signal levels, compared with those made with the ribbon bonds to sources.

These devices, however, had one problem in the packing density of the FET pattern. Namely, these devices needed a wide source-electrode segment of 50 μm since each via-hole was made by a chemical etching technique which introduced large lateral etching. Therefore, these via-connection structures could not be applied to high-frequency devices, such as *K*-band devices, because the FET chip size in higher frequency would become small and the source-electrode having the width of 50 μm could not be designed.

Recently, the plasma-etched via-connections technique to GaAs FET's has been developed [5]. This technique can produce vertical walls with negligible lateral etching under the photoresist mask. This capability allows the design of devices with higher packing density than the wet chemical-etching technique. It could produce a 100-percent increase in electrode packing density in comparison with the chemical-etching technique. Even this plasma-etching technique, however, needs a via-hole diameter of 12 $\mu m\phi$ and a source-electrode segment width of 32 μm [5].

Although this degree of packing density in FET patterns is valuable for low-frequency devices such as in *L*- and *C*-band which have large chip sizes, it may be not valid for high-frequency devices which are not permitted to have the source-electrode segment width more than several micrometers. A more sophisticated via-hole connection-structure should be developed for *K*-band GaAs power FET's.

In this paper, the design consideration for high-frequency GaAs power FET's, such as in *K*-band, is discussed and the limitations in the active area size are derived. In Section III, a novel Via-Hole PHS structure is developed to design a *K*-band GaAs power FET under these limitations [6]. The source-inductance of the novel Via-Hole PHS FET is assessed in comparison with that of a sheet-grounded FET[1] and a conventional direct via-hole PHS FET (in Section IV). The RF performances at 20 GHz and 30 GHz for chip-carrier devices are reported (in Section V), and in addition, the same device assembled into a hermetically sealed package is evaluated at 20 GHz (in Section VI). Finally, thermal- and mechanical-environmental tests for 2.4-mm gate periphery FET's are made.

II. DESIGN CONSIDERATIONS FOR A LARGE GATE PERIPHERY FET

A. Gain Degradation with the Increase of the Gate Periphery

It is generally known that a power FET is composed of a number of small-signal FET unit cells, and the gate periph-

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[1]The sheet-grounded FET is Fujitsu's conventional device which is grounded by soldering the vertical plane of the longer side in the FET chip with AuSn. The thickness of the substrate is 70 ~ 80 μm.

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ery of one unit cell is several hundred micrometers, and that of a power FET chip is from 1–10 mm. However, it is also general that the gain in a high-power FET with a several-millimeters gate periphery is smaller by a few decibels than that in the unit cell at the same input power levels per unit gate periphery. The gain in a large gate periphery FET should essentially be the same as that in the unit cell. What is the origin of this gain degradation?

We consider that the gain degradation in the FET with a large gate periphery is caused by the following four problems:

1) phase-unbalance of the incident wave at gate-bonding pads due to the variation of gate-bonding wire-length,
2) increase in matching losses due to increased impedance ratio of matching circuits,
3) increased nonuniformity in the channel temperature distribution of larger gate FET's,
4) out of phase operation between unit cells due to lack of uniformity in the active layer (both material- and process-variation).

The gain degradation concerning problems 1) and 2) can be considerably improved using circuit techniques such as the internally matching technique [7] or the inphase divider/combiner technique [8]. However, the devices matched by these techniques inevitably have a fixed frequency band, and so, these cannot be used in the general application.

Problem 3) can be solved by thining the substrate, which can be made easily as a by-product of the via-hole PHS structure.

Problem 4) is the most troublesome. The solution for this is presently considered to be the extreme reduction in the length of the active area of a power FET. It may be noted that this length should become smaller with increasing frequency, as well as the unit gate width [9]. Also, problem 1) can be solved by the reduction in the length of an FET active area because the number of the bonding pads can be decreased. From these reasons, it is concluded that the via-hole FET with the very thin substrate and the very small length of an active area can solve problems 1), 3), and 4). The best solution for problem 2) may be the monolithic integrated circuit.

B. Limitation in the Length of an FET Active Area

The relationship between the length of an FET active area L and the wavelength λ at an operating frequency has not been discussed at all. No analytical method to determine the length L has been reported to date. Therefore, in this paper, a design chart for the length of an FET active area L is proposed, which was roughly determined on the basis of the lumped element consideration (Fig. 1).

The FET pattern, such as a unit gate width, has been generally designed on the basis of the lumped element consideration [9]. For example, a unit gate width is determined to be one-tenth of the length which the phase angle of an input signal shifts $\pi/4$ rad. Therefore, the unit

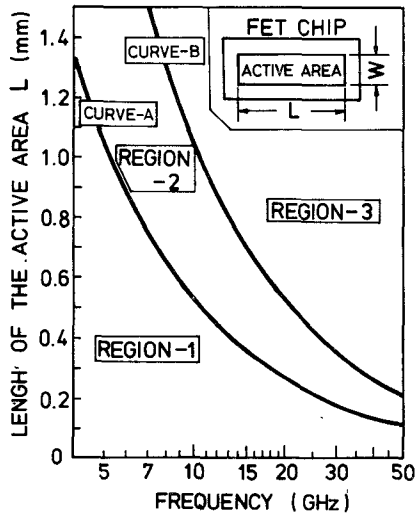

Fig. 1. Design chart for the length of an FET active area L. As shown in the insert, the length L is the longer side of an active area and is perpendicular to the direction to which RF signals proceed. Two curves, A and B, divide the design chart into three regions. When the length of an active area is designed to be in region 1 (for example, no longer than 0.5 mm at 10 GHz), the length L can be considered as a lumped element at the frequency and all the unit cells in the chip will operate inphase. When the length L is in region 3 (no smaller than 1.0 mm at 10 GHz), it cannot be regarded as a lumped element, and so some sophisticated circuit technique (such as the inphase divider/combiner technique) is needed for the successful operation of the FET chip. Region 2 means that the gain degradation may appear but is not so large. It can be said from the point of view of the FET chip design that in region 1 its design is good, in region 3 it is poor, and in region 2 it is acceptable.

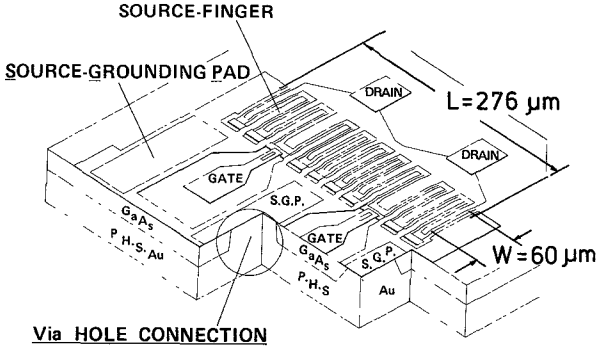

Fig. 2. Cross-sectional view of a K-band 1.2-mm gate periphery GaAs FET with the novel Via-Hole PHS structure. The source-grounding pads which are fabricated outside the active area are directly connected to the PHS through the holes made under these pads. The active area is 0.06×0.276 mm, and the ratio of gate periphery to active area (W_g/S_a) is 66 mm^{-1}.

gate width can be considered as a lumped constant element. The length of an active area L should be determined to be one-second of $\pi/4$ rad, that is, to be $1/16 \cdot \lambda$, because if two gate-bonding pads[2] in the span of $1/16 \cdot \lambda$ are permitted to be designed as shown in Fig. 2, the maximum phase-shift angle of an input signal along the direction of the length L is calculated $\pi/32$ rad, which is nearly equal to a unit gate width.

[2]In the frequency lower than C-band, the FET chip may be able to have more gate-bonding pads because problem 1) is not so serious.

Fig. 1 shows the design chart for the length of an FET active area L. As shown in the insert in this figure, the length L and width W of an active area are defined as follows: The length L is the longer side of an active area and is perpendicular to the direction to which RF signals proceed, and the width W is the shorter side of the active area and is the same as the unit gate width W_u. Two curves, A and B, in this figure correspond to the length of $1/16 \cdot \lambda$ and $1/8 \cdot \lambda$ on GaAs substrate, respectively. These two curves divide the design chart into three regions. When the length of an active area in an FET chip is designed to be in region 1 (for example, no longer than 0.5 mm at 10 GHz), the length L can be considered as a lumped element at the frequency. In the FET chip having such a length L, it is expected that problems 1), 3), and 4) will not be serious and all the unit cells in the chip will operate inphase.

On the other hand, when the length L is in region 3 (no smaller than 1.0 mm at 10 GHz), it cannot be regarded as a lumped element, and so some sophisticated circuit techniques, such as the inphase divider/combiner technique mentioned above, are needed for the successful operation of the FET chip. Region 2 means that the gain degradation may appear but it is not so large. Consequently, it can be said from the point of view of the FET chip design that in region 1, its design is good, in region 3 it is poor, and in region 2 it is acceptable.

From this figure, the length of an active area L is determined to be about 0.27 mm at 20 GHz. The unit gate width W_u at 20 GHz can be calculated to be about 60 μm by using [9]. A set of these two values is the limitation on designing a K-band power FET pattern.

III. Novel Via-Hole Structure

In the design of power FET's, it should be taken into consideration how a large total gate periphery can be designed within the limitations obtained in the previous section. For example, let us consider the design of an FET whose saturation power is 0.5 W. This half-watt FET will need the total gate periphery of 1.2 mm, which corresponds to the device which has the capability of 0.42-W power output per millimeter gate periphery. Such an FET design is quite possible. In this design, next, the number of gate fingers can be determined to be 20, since the unit gate width W_u is 60 μm. Therefore, the width of a source-electrode segment can be calculated to be 6 μm in case of the drain–source distance of 5 μm. It is impossible to make a via-hole just underneath such a narrow source-electrode segment. Therefore, a more sophisticated via-hole structure, a novel Via-Hole PHS structure has been developed.

Fig. 2 shows the cross-sectional view of a K-band 1.2-mm gate periphery GaAs FET with the via-hole PHS structure. The source-grounding pads fabricated outside the active area are directly connected to the PHS through the holes made under these pads. The dimensions of the active area finally determined are 0.060×0.276 mm, as shown in Fig. 2.

Let us introduce a new parameter, a ratio of total gate periphery to active area ($= W_g/S_a$), which indicates how the large total gate periphery can be designed within the limitations of the active area size ($L \times W$) given above. The (W_g/S_a) ratio in the FET designed is 66 mm^{-1}, which is about four times as much as that in the conventional direct via-hole structure device reported so far [8].

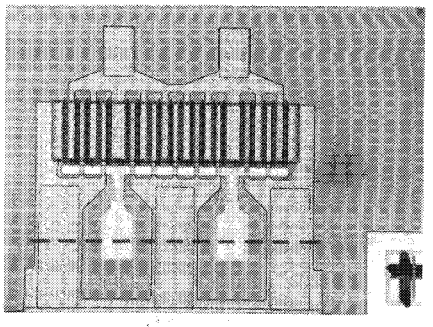

Fig. 3. Top view of the completed novel Via-Hole PHS FET with a 1.2-mm gate periphery.

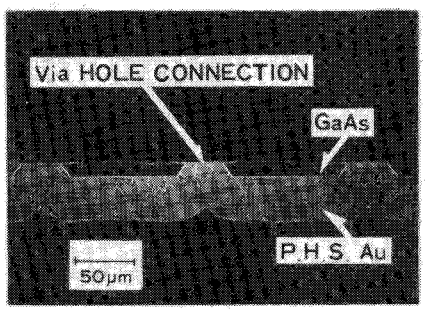

Fig. 4. Scanning electron microscopy photograph of the cross-sectional view of the completed novel Via-Hole PHS FET. The cut line is shown with a dotted line in Fig. 3. The thickness of the GaAs substrate and the PHS in this sample are about 10 μm and 35 μm, respectively. The width of a source-grounding pad is designed to be 53 μm and the bottom width of a via-hole was made to be about 35 μm in this sample.

It is natural that the source-inductance L_s of this novel Via-Hole FET will become larger than that of the conventional via-hole FET. The increment in the source-inductance ΔL_s, however, can be estimated to be, at most, several picohenries as discussed in Section IV, which is thought to have no detrimental effect on the RF performance up to K-band. Fig. 3 shows the top view of the completed novel Via-Hole PHS FET with a 1.2-mm gate periphery.

The scanning electron microscopy photograph of the cross-sectional view of the completed novel Via-Hole PHS FET is shown in Fig. 4. The cut line is shown with a dotted line in Fig. 3. The thickness of the GaAs substrate in this sample are about 10 μm, although the average value is 20 μm. The width of a source-grounding pad is designed to be 53 μm and the bottom width of a via-hole was made to be about 35 μm in this sample. This cross-sectional-view photograph illustrates that the bottom width of a via-hole can be as large as 53 μm. This large etching tolerance is also one of the features of this novel Via-Hole structure.

IV. Source Inductance in the Novel Via-Hole FET

It is important to measure the source-inductance of the completed device in order to appreciate the newly devel-

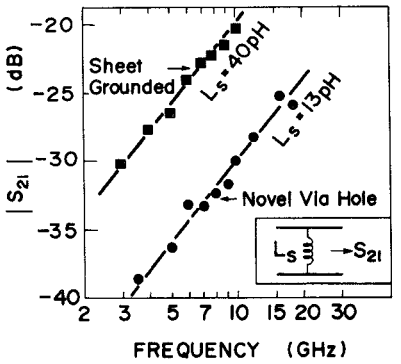

Fig. 5. Source-inductances L_s calculated from measured $|S_{21}|$ of the FET's whose active areas are shorted with gold sheets. From this figure and equation $S_{21} = 2/Z_0 \cdot L_s \cdot j\omega$, the source-inductance for the novel Via-Hole FET and for the sheet grounded FET[1] can be obtained to be 13 pH and 40 pH, respectively.

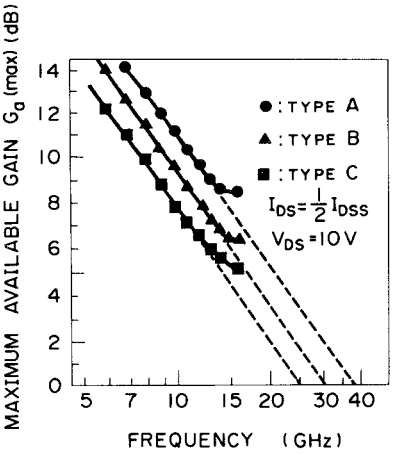

Fig. 6 Frequency dependence of the maximum available gain G_a(max) calculated from measured S-parameters for three types of 1.2-mm gate periphery devices. The type A and B devices are the novel Via-Hole PHS FET with 0.7- and 1.0-μm gate length, respectively. The type C device is the sheet-grounded FET with 1.0-μm gate length, which has no via-hole structure.

oped Via-Hole structure. However, it is very difficult to measure directly the source-inductance of the completed device because the value of the inductance is extremely small. Therefore, the source inductance of the completed device was measured by the following method. 1) The source- and drain-electrodes in the active area of the completed FET are shorted with a gold sheet which has almost the same size as that of the active area of the FET. 2) The sample is interconnected from both input- and output-transmission lines with a gold ribbon which has almost the same width as the microstripline width. In this case, the width is 300 μm, which coincides with that of the sample. 3) Then, the equivalent circuit can be expressed as shown in the insert in Fig. 5, where L_s means the existence of the inductance between the source-electrodes and the plated heat sink metal, and this L_s is the source-inductance of the FET.

When the circuit is terminated with the characteristic impedance Z_0, the S-parameter S_{21} can be given by [10]

$$S_{21} = 1 - \frac{y}{y+2} \tag{1}$$

where $y = Z_0/j\omega L_s$, $\omega = 2\pi f$, $Z_0 = 50\ \Omega$. Since the value of L_s is the order of several tens of picohenries, $\omega L_s \ll Z_0$ holds for frequencies below 20 GHz. Therefore, (1) is approximated by

$$S_{21} = \frac{2}{Z_0} \cdot L_s \cdot j\omega. \tag{2}$$

Thus, the inductance L_s can be obtained from the gradient of $|S_{21}|$ versus frequencies.

Fig. 5 shows the measured S-parameter $|S_{21}|$ versus frequencies. From this figure and (2), the source-inductances for the novel Via-Hole FET and for the sheet grounded FET[1] can be obtained to be 13 pH and 40 pH, respectively. It is clear that the source-inductance L_s of the novel Via-Hole FET is improved by about one-third than that of the sheet grounded FET.

Although there has been no report so far that the source-inductance L_s of conventional, direct via-hole FET's has been theoretically calculated and directly measured, it can be estimated to be a few picohenries from the data on the RF performance reported by D'Asaro *et al.* [4] in the case of 3-mm gate periphery FET's. Therefore, the increment in the source-inductance of novel Via-Hole FET's ΔL_s, compared with conventional via-hole FET's, is calculated to be several picohenries per millimeter gate periphery.

V. RF Performance

A. Small Signal

Fig. 6 shows the frequency dependence of the maximum available gain G_a(max) calculated from measured S-parameters for three types of 1.2-mm gate periphery devices. The type A and B devices are the novel Via-Hole PHS FET with 0.7- and 1.0-μm gate lengths, respectively. The 0.7-μm gate was defined with the new technique in the direct electron-beam lithography, which can define the gate length and the recess-configuration accurately and simultaneously [11]. The type C device is the sheet-grounded FET[1] with a 1.0-μm gate length, which has no via-hole structure.

Compared with type C, the G_a(max) of type B is larger by a factor of 1.7 dB. This comparison includes both the reduction of the source-inductance and the thermal-resistance by the novel Via-Hole structure. Moreover, the reduction from 1.0 μm to 0.7 μm in the gate length resulted in the increase of 1.5 dB in G_a(max).

It is found that by extrapolating G_a(max) at lower frequencies a linear gain G_1 of more than 5.5 dB at 20 GHz can be expected from the type A device.

It is well known that the maximum available gain G_a(max) decreases at the rate of 6 dB/octave with increasing frequency, which generally can be expressed in the following useful approximation [9]:

$$G_a(\max) = \left(\frac{f_t}{f}\right)^2 \cdot \frac{1}{4g_{ds}(R_g + R_i + R_s + \pi f_t L_s) + 4\pi f_t C_{dg}(2R_g + R_i + R_s + 2\pi f_t L_s)} \tag{3}$$

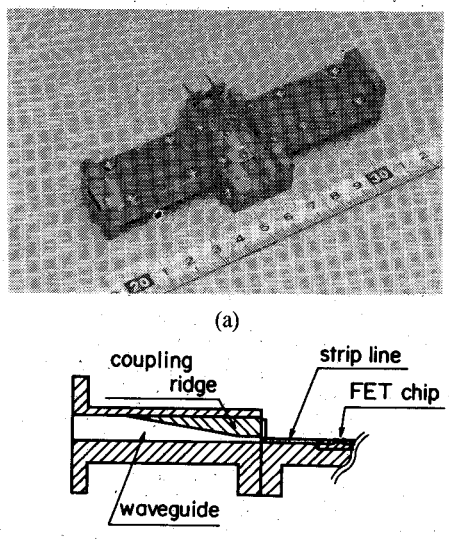

Fig. 7. (a) The 20-GHz RF test fixture. The waveguide is the WRJ-220. The sample mounted into the test fixture in this photograph is a packaged 20-GHz 1-W novel Via-Hole PHS FET. (b) Schematic of the stripline–waveguide transition in this test fixture.

where f_t is the cutoff frequency, f is the operating frequency, g_{ds} is the drain conductance, R_g is the gate series resistance, R_i is the channel resistance between source and gate, R_s is the source series resistance, L_s is the source-inductance, and C_{dg} is the drain-to-gate capacitance.

In higher frequencies, however, the rate becomes less steep. For example, it is calculated by using the computer simulation that the rate will become 3 dB/octave or less [12], [13]. The precise observation on the data plotted in Fig. 6 makes us realize that this calculation may be correct. Then, it can be expected that the type A device will exhibit a linear gain G_1 of more than 4 dB at 30 GHz.

B. Large Signal

Fig. 7(a) shows the 20-GHz RF test fixture which has the stripline–waveguide transition as shown in Fig. 7(b). The waveguides used were the WRJ-220 system for 2-GHz measurements and the WRJ-320 system for 30-GHz measurements.

Fig. 8 shows that output power and the power added efficiency versus the input power both at 20 GHz and 30 GHz for the type A device, which has the novel Via-Hole structure and a 0.7-μm gate length. The FET chip is assembled on a chip-carrier. The output power at 0.63 W (28 dBm) with 5-dB gain and 20-percent power added efficiency at 20 GHz, and the 0.5 W (27 dBm) with 4-dB gain and 14-percent efficiency at 30 GHz were obtained. The linear gain at 20 GHz and 30 GHz were 6.1 dB and 4.6 dB, respectively. The typical thermal resistance of this device was measured 26°C/W using an IR scanning method, and the channel temperature rise ΔT_{ch} at the point of output power 28 dBm at 20 GHz could be estimated to be about 30°C. These data show that the type A device with 1.2-mm gate periphery may be applicable to both 20-GHz and 30-GHz practical uses.

As predicted above, the difference in the linear gain G_1 between 20 GHz and 30 GHz is smaller than that calculated by (3). It may be noted that (3) cannot be valid in higher frequencies.

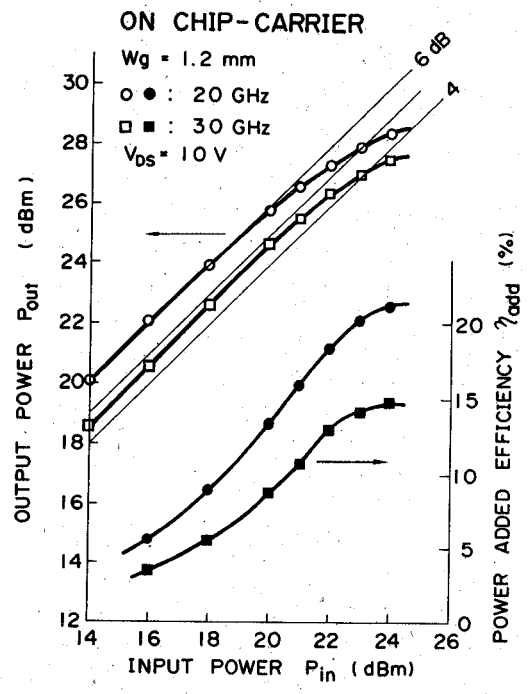

Fig. 8. Output power and power added efficiency versus input power both at 20 GHz and 30 GHz for the 1.2-mm novel Via-Hole PHS FET with a 0.7-μm gate. The FET chip is assembled on a chip-carrier. The thermal resistance of this device is 26°C/W and the channel temperature rise ΔT_{ch} at the point of output power 28 dBm at 20 GHz is estimated to be about 30°C.

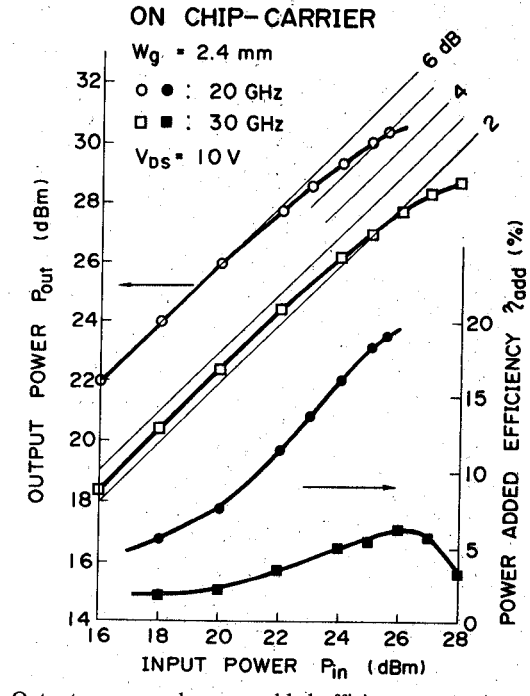

Fig. 9. Output power and power added efficiency versus input power both at 20 GHz and 30 GHz for the 2.4-mm novel Via-Hole PHS FET with a 0.7-μm gate. The FET chip is assembled on a chip-carrier. The channel temperature rise ΔT_{ch} is 38°C at the point of output power 30 dBm at 20 GHz (the thermal resistance is 13°C/W).

The same device as the type A, except that the gate periphery was twice ($W_g = 2.4$ mm), was fabricated. The active area size of this device is 0.060×0.529 mm, which

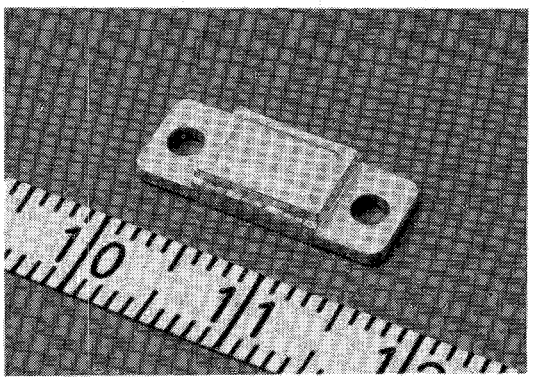

Fig. 10. A 20-GHz hermetically sealed package. This package is composed of metal blocks except the 50-Ω coaxial line where RF signals and dc bias supplies pass through.

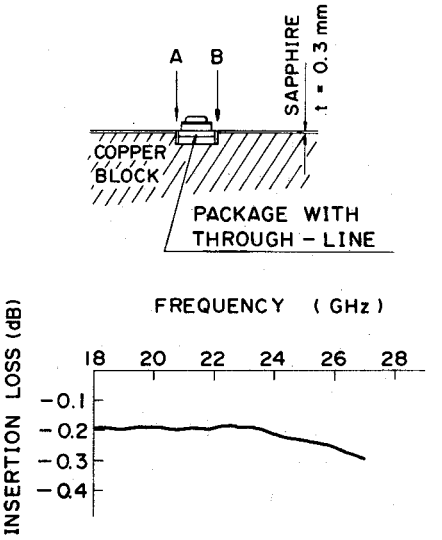

Fig. 11. Measured insertion losses of the 20-GHz hermetically sealed package. The measurement was made with the package which had a "through 50-Ω line" fabricated on the 0.3-mm sapphire substrate.

satisfies the "acceptable condition" at 20 GHz, and corresponds to the "poor design" at 30 GHz in the design chart of Fig. 1. Therefore, it is expected that this device will be able to deliver the acceptable RF performance at 20 GHz, but will show the poor output power at 30 GHz.

Fig. 9 shows the output performances of this device assembled on a chip-carrier. At 20 GHz, the output power at 1.1 W (30.4 dBm) was obtained with a 4.9-dB gain and 19.2-percent power added efficiency, when the channel temperature rise ΔT_{ch} was 38°C (the thermal-resistance is 13°C/W). On the other hand, at 30 GHz, the output power 28.7 dBm was achieved with 0.7-dB gain and 3.2-percent power added efficiency. The maximum efficiency was 6.2 percent at the output power of 27.8 dBm. The linear gain at 20 GHz and 30 GHz were 6 dB and 2.4 dB, respectively.

These degraded results at 30 GHz mean that in order to get good RF performance at 30 GHz from this device, some sophisticated matching circuit techniques should be applied, as described in Section II.

VI. A Packaged 20-GHz 1-W Device

The same novel Via-Hole PHS FET chip as used in the experiment in Fig. 9 was packaged with a hermetic seal. This package is composed of metal blocks except the 50-Ω coaxial line where RF signals and dc bias supplies pass through, as shown in Fig. 10 [14]. Fig. 11 shows the measured insertion losses between terminals A and B in the frequency range from 18 to 27 GHz. The measurement was made with the package which had a "through 50-Ω line" fabricated on the 0.3-mm sappire substrate. The results show that no self-resonance was observed up to 27 GHz and the insertion loss was less than 0.2 dB at 20 GHz. This packaged device mounted into the 20-GHz test fixture is shown in Fig. 7(a).

Fig. 12 shows the RF performance of the packaged novel Via-Hole PHS FET at 20 GHz. The output power 1.0 W (30 dBm) with 4.8-dB gain and 13.1-percent power added efficiency was obtained. These data also show that even at 20 GHz, the space-qualified packaged GaAs FET's [15] can be produced in the production level.

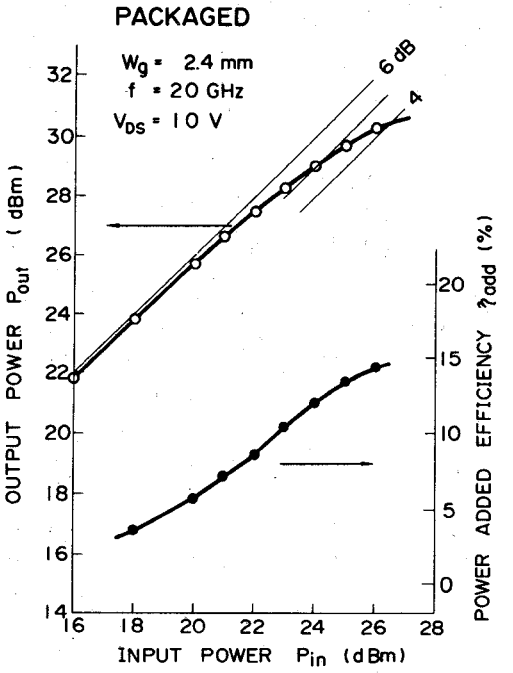

Fig. 12. Output power and power added efficiency versus input power at 20 GHz for the packaged 2.4-mm novel Via-Hole PHS FET with a 0.7-μm gate. Also, these data show that even at 20 GHz, the space-qualified packaged GaAs FET's [15] can be produced in the production level.

VII. Reliability

The PHS structure has been introduced for high-power, high-reliability GaAs FET's. For example, Fukui *et al.* [16] reported that from RF- and dc-life tests of a total of 265 conventional PHS 6-mm-wide devices, the failure rate for burnout at a maximum channel temperature in normal operation of 110°C would be expected to be below 100 FIT's. Therefore, this paper will concentrate on the problems characteristic of via-hole PHS FET's.

TABLE I
TEST PARAMETERS, MEASUREMENT CONDITIONS, INITIAL VALUES, AND FAILURE CRITERIA IN THE THERMAL AND MECHANICAL TESTS FOR NOVEL VIA-HOLE PHS FET'S

Test parameters	Measurement conditions	Initial value			Failure criteria (Percent change)	
		Typ.	Std. dev.	Unit	Min.	Max.
I_{GSS}	V_{GS}=-2V, V_{DS}= 0V	0.04	0.02	μA	—	+100
I_{DSS}	V_{GS}= 0V, V_{DS}= 5V	540	68	mA	-10	+ 10
V_P	V_{DS}= 5V, I_{DS}=20mA	-2.7	0.83	V	-10	+ 10
g_m	V_{DS}= 5V, I_{DS}=300mA	210	11	mS	-10	+ 10
P_o	V_{DS}= 9V, I_{DS}= I_{DSS}/2 f = 12.0 GHz P_{in}=+20 dBm	27	0.5	dBm	-1 dB	+1 dB

TABLE II
TEST CATEGORY, TEST CONDITIONS, AND RESULTS. THROUGHOUT TESTS, NO FAILURE NOR SIGNIFICANT PARAMETER'S PERCENT CHANGE WAS OBSERVED

Test Group	Test Category	MIL-STD-750 Method	Test Methods and Conditions	Sample Size	Acceptance Number	Results Number of Failed
Thermal	Soldering Heat	2031	260°C, 10sec, 1 cycle	8	0	0
	Temperature Cycling	1051	(MIL-STD-202C Method 107B) cond 100 cycle -65°C, 25°C, +200°C, 30min	8	0	0
	Thermal Shock	1056	0°C, +100°C, 5min, 5 cycle	8	0	0
Mechanical	Shock	2016	Orientation X, Y, Z, 3 cycle 1500G, 0.5ms	8	0	0
	Vibration, Variable Frequency	2056	Orientation X, Y, Z 4cycle 100-2000Hz, 20G, 4min	8	0	0
	Constant Acceleration	2006	20,000G, X, Y, Z 1min	8	0	0

Compared with the conventional PHS FET, the via-hole PHS FET has the following two different structures: 1) several holes fabricated through the buffer and the substrate and 2) the thinner substrate (about one half, 20 μm). A concern in such via-hole structures is that cracks may be introduced in the GaAs substrate in the surrounding area of these holes because of thermal- and mechanical-deformation stresses in actual applications. To estimate the environmental reliability for the newly developed novel Via-Hole PHS FET's, several kinds of thermal and mechanical tests were made.

Test parameters, measurement conditions, initial values, and failure criteria are listed in Table I. The samples used in this test were 2.4-mm gate periphery novel Via-Hole PHS FET's with the die size of 0.45×0.75 mm. All these chips were assembled into hermetically sealed ceramic packages. In the RF test, a frequency of 12 GHz was chosen for test because of convenience. Samples were divided into two test groups: 1) thermal environment and 2) mechanical environment.

Test category, test conditions, and test results are summarized in Table II. Test items are those commonly used for a highly reliable semi-conductor based on MIL-Standards. Extreme heat cycles were applied to the samples (as much as 100 cycles).

Throughout these thermal and mechanical tests, any failure exceeding the parameter's percent change in Table I was not observed as shown in Table II. From this result, it can be concluded that the novel Via-Hole PHS FET with a thin substrate of 20 μm is able to endure most of the serious circumstances and will be feasible as a highly reliable device.

VIII. CONCLUSION

The novel Via-Hole PHS structure for *K*-band GaAs power FET's has been developed. This structure has the gate periphery to active area ratio (W_g/S_a) of 66 mm^{-1}. This ratio indicates the gate-packing ability, which is one of the most important design factors in high-power FET's.

Compared with the conventional direct via-hole FET's, the increment in the source-inductance of the novel Via-Hole PHS FET's, ΔL_s has been estimated to be several picohenries per millimeter gate periphery. It has been expected that such a small value of the source inductance had little effect on RF performance at 20 GHz. In fact, the completed novel Via-Hole PHS FET with a 0.7-μm gate length and a 1.2-mm gate periphery, delivered output powers of 28 dBm at 20 GHz with 5-dB gain, 20-percent power added efficiency, and 30°C channel temperature rise, which were significant data for the practical use at 20 GHz.

The 2.4-mm gate periphery device also with the novel Via-Hole PHS structure exhibited output power of 30.4 dBm at 20 GHz with 5.0-dB gain, 19.2-percent power added efficiency, and 38°C channel temperature rise, while the same device yielded an output power of 28.7 dBm at 30 GHz with 0.7-dB gain and 3.2-percent power added efficiency. These degraded results at 30 GHz suggest that the 2.4-mm gate periphery device should be redesigned on the basis of a "design chart for the length of an active area," proposed in this paper, so that it might exhibit significant data at 30 GHz.

The 2.4-mm gate FET assembled in the hermetically sealed package delivered 30-dBm output power at 20 GHz with 4.8-dB gain and 13.1-percent power added efficiency. Also, these data have shown that even at 20 GHz, the space-qualified packaged GaAs FET's can be produced in the production level.

The reliability test results for the novel Via-Hole PHS FET's have been described. Especially, thermal- and mechanical-shock tests have been discussed and have been made with the MIL-STD-750 method. As a result, no failure mode has been observed and the novel Via-Hole PHS FET's have been proved to be feasible as a highly reliable device.

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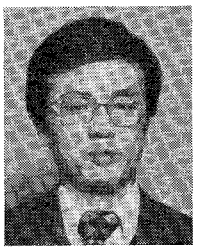

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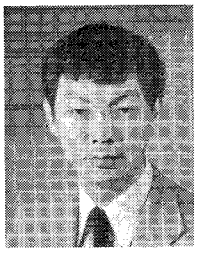

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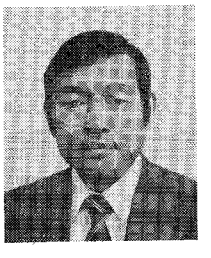

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